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Flexible Low-Voltage Organic Thin-Film Transistors Enabled by Low-Temperature, Ambient Solution-Processable Inorganic/Organic Hybrid Gate Dielectrics

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Abstract: We report here on the design, synthesis, processing, and dielectric properties of novel cross-linked inorganic/organic hybrid blend (CHB) dielectric films which enable low-voltage organic thin-film transistor (OTFT) operation. CHB thin films (20−43 nm thick) are readily fabricated by spin-coating a zirconium chloride precursor plus an α,ω-disilylalkane cross-linker solution in ambient conditions, followed by curing at low temperatures (~150 °C). The very smooth CHB dielectrics exhibit excellent insulating properties (leakage current densities ~10^{-7} A/cm^2), tunable capacitance (95−365 nF/cm^2), and high dielectric constants (5.0−10.2). OTFTs fabricated with pentacene as the organic semiconductor function well at low voltages (<−4.0 V). The morphologies and microstructures of representative semiconductor films grown on CHB dielectrics prepared with incrementally varied compositions and processing conditions are investigated and shown to correlate closely with the OTFT response.

Introduction

Organic thin-film transistor (OTFT)-based electronics performing simple operations offer unique attractions compared to conventional inorganic technologies, including low cost, large-area coverage, and low processing temperatures suitable for flexible substrates.[1] A typical bottom-gate top-contact OTFT structure is shown in Figure 1A. In this device architecture, the current between the source and the drain contact is modulated by both the source−drain voltage (V_{SD}) and the source−gate voltage (V_G). When the device is in the off state ($V_G = 0.0$ V), the channel current must be very low, whereas in the on state of the source−gate voltage relationship ($V_G \neq 0.0$ V), large, abrupt current increases must be achieved. The saturation current in organic thin-film transistors is generally described by the following equation:

$$I_{DS} = \frac{W}{2L}\mu C_i (V_G - V_T)^2 \quad (1)$$

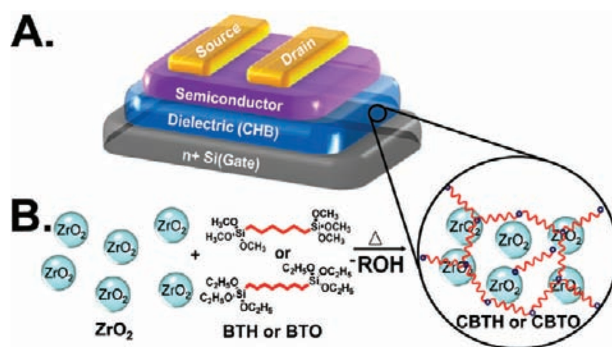

Figure 1. (A) Schematic of a bottom-gate/top-contact OTFT device geometry and the dielectric layer employed in this study. (B) Chemical structures of the ZrO_2 and siloxane cross-linkers employed and the CHB dielectric densification process.

where μ is the field-effect charge carrier mobility, C_i is the capacitance per unit area of the dielectric, V_T is the threshold voltage, and W and L are the OTFT channel width and length, respectively. Despite recent impressive progress in developing new organic semiconductors,[2] large OTFT operating voltages, reflecting the intrinsically low mobilities of organic versus conventional inorganic semiconductors, remain one of the major challenges to overcome.[3] For low-power applications such as RF-ID tags, flat panel displays, and portable electronics, it is

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mandatory to achieve high thin-film transistor (TFT) drain currents (I_{SD}) at acceptably low operating voltages. Without changing the device geometry (W and L) and semiconductor material (μ), equivalent OTFT I_{SD} parameters should be achievable at lower operating voltages by increasing the gate dielectric capacitance C_i, given by the following equation:

$$C_i = \varepsilon_0 \frac{k}{d} \qquad (2)$$

where ε_0 is the vacuum permittivity, k the dielectric constant, and d the thickness of the dielectric layer.

From eq 2, note that operating bias reduction can be achieved by either increasing the dielectric constant (k) or decreasing the thickness (d) of the gate dielectric layer. An increase in the k/d ratio is also essential for efficient device scalability, a prerequisite to enhancing low-power TFT operation. In addition to an increased k/d ratio, it is also necessary for the gate dielectric to be processable from solution and at low temperatures to enable compatibility with flexible plastic substrates and circuitry production via roll-to-roll and related fabrication technologies. To date, cross-linked polymer films, metal oxides, polymer/high-k nanoparticle composites, and hybrid inorganic/organic dielectrics are proven candidates for low-voltage TFTs.[4−7] However, all of these materials have some limitations in achieving practical, flexible, low-voltage TFTs. First, cross-linked polymeric materials typically have relatively low k values, and thus, TFT drain currents (I_{SD}) at low operating voltages are frequently insufficient.[4] An alternative approach is to employ high-k materials such as metal oxide (MO) films.[5] However, high-quality MO dielectric films typically require high growth/annealing temperatures (>400 °C) and/or vacuum deposition (e.g., atomic layer or chemical/physical vapor deposition) to ensure acceptably low leakage currents. Furthermore, most high-k metal oxide films, particularly the polycrystalline ones, are too brittle for flexible electronics applications. Another strategy to increase the k/d ratio and mechanical flexibility is to use polymer/high-k inorganic nanoparticle composites.[6] However, the dielectric constants of these composite materials are generally dominated by the relatively low-k polymeric component. To increase composite k values, large nanoparticle loadings are necessary; however, this generally results in greatly enhanced surface roughness and poor mechanical flexibility. Last, hybrid gate dielectrics composed of self-assembled monolayers or multilayers containing ultrathin inorganic oxides show promise for low-voltage OTFTs;[7] however, low-cost pathways for integration into large-volume coating processes are still under development.

To address the above issues, optimum gate dielectric films should have high k values and good insulating properties and be fabricable via solution-processing techniques at low temperature under ambient conditions. Here we report a new class of cross-linked inorganic/organic hybrid blend dielectric materials (Figure 1B) compatible with plastic substrates and deposited via a solution-phase process, which affords high gate capacitances, low leakage current densities, and smooth surfaces when integrated into TFT structures. In addition to very large dielectric strength, the combined properties of both soft-matter and hard-matter components enables these new materials to be mechanically flexible and thermally/environmentally robust. Furthermore, these densely cross-linked hybrid blends ensure that subsequent device layers can be solution-processed without dissolution of the dielectric layer.

The new composites are based on high-k zirconium oxide (k = 16−25)[8] as the inorganic component, derived from commercially available $ZrCl_4$. Note that zirconium oxide has a wide band gap (5.8 eV),[9] which is potentially useful for transparent device applications. The organic component of this hybrid gate dielectric is an α,ω-disilylalkane cross-linking agent. Spin-coated formulations of these two components result in dielectric films exhibiting high k values (5−10), high capacitances (95−365 nF/cm^2), and low leakage current densities (4×10^{-7} to 6×10^{-6} A/cm^2 at 2 MV/cm). Furthermore, it will be shown that these dielectrics function far more effectively than neat ZrO_x films which are fabricated in parallel for control experiments. Finally, pentacene OTFTs fabricated on plastic substrates with these new hybrid dielectrics are shown to operate at low voltages

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(<−4.0 V) and to offer high on/off current ratios (>10^5) as well as substantial hole mobilities (0.2−1.5 $cm^2/(V\cdot s)$).

Experimental Section

Materials. The precursors for the present dielectric films were prepared using zirconium(IV) chloride (99.5%, Aldrich) plus 1,6-bis(trimethoxysily)hexane (98%, Gelest) or 1,8-bis(triethoxysily)-octane (98%, Gelest). Heavily n-doped Si wafers (Montco Silicon Tech) for gate electrodes were cleaned according to standard procedures. Aluminum was deposited on Kapton (Dupont) as a gate electrode for flexible devices. Pentacene for the p-type organic semiconductor was commercially available and was purified by published procedures.[4b] Multiple high-vacuum temperature gradient sublimed PDIF-CN_2 from Polyera Corp. was chosen as the n-type organic semiconductor.

Dielectric Film and OTFT Fabrication. An absolute ethanol solution (0.10 M) in zirconium(IV) chloride was prepared, followed by the addition of a mixture of nitric acid and deionized (DI) water (molar ratio $ZrCl_4$:HNO_3:H_2O = 1:10:10). The resulting zirconium precursor solution was then heated to 50 °C for 3 h to accelerate hydrolysis. For the control zirconium oxide (ZrO_2) film fabrication, the above zirconium precursor solution was spin-coated onto substrates at 5000 rpm for 30 s and then cured at a temperature of 150, 300, 400, or 500 °C for 1 h. For cross-linked inorganic/organic hybrid blend (CHB) film fabrication, 0.10 M 1,6-bis(trimethoxysily)hexane or 1,8-bis(triethoxysily)octane solutions in EtOH, referred to in the rest of this paper as BTH and BTO, respectively, were added to the hydrolyzed zirconium chloride solution in a 1:0.5, 1:0.2, or 1:0.1 $ZrCl_4$:cross-linker molar ratio. These solutions were then spin-coated at 5000 rpm for 30 s, followed by curing in a vacuum oven at 150 °C for 2 h. All dielectric precursor solutions were filtered through a 0.2 μm pore size PTFE membrane syringe filter prior to spin-coating and were spin-coated under a controlled atmosphere of less than 10% relative humidity (measured with a Fisher Scientific traceable hygrometer−thermometer−dew point probe). Before dielectric layer deposition, the heavily doped n^+-silicon (Montco Silicon Technologies, Inc.) substrates were cleaned in EtOH (Aldrich, absolute, 200 proof) by sonication for 2 min and then dried under flowing nitrogen, followed by oxygen plasma treatment for 5 min to remove organic contamination and to improve the wettability. After dielectric layer deposition, bottom-gate/top-contact OTFTs were completed by vacuum deposition of pentacene (50 nm, 5×10^{-6} Torr, 0.05 nm/s growth rate) onto each ZrO_2- and CHB-dielectric-coated substrate, followed by gold source (S)−drain (D) electrode vacuum deposition (50 nm, 0.02 nm/s growth rate) through a shadow mask to yield S−D contacts of dimensions L = 100 μm and W = 2000 μm. For metal/insulator/semiconductor (MIS) test structures, gold electrodes of dimensions 200 μm × 200 μm were deposited directly onto the Si−gate dielectric films through a shadow mask. Flexible OTFTs were fabricated using a top-contact geometry on plastic substrates (Kapton). Thus, aluminum was thermally evaporated onto the Kapton films as the gate electrode, and the CHB gate dielectric and a 50 nm thick pentacene semiconducting layer were then deposited onto the aluminum layer as described above. Gold was thermally evaporated onto the pentacene films through a shadow mask to define the source and drain electrodes. These OTFTs had a channel length of 100 μm and channel width of 2000 μm.

Dielectric Film and OTFT Characterization. The film thicknesses of the ZrO_2 dielectric films after annealing at different temperatures were analyzed by X-ray reflectivity (XRR), and glancing incidence X-ray diffraction (GIXRD) scans were measured on a Rigaku ATX-G thin-film diffraction workstation using Cu Kα radiation. The thermal stability of the CHB precursors was assessed using a Shimadzu TGA-50 thermogravimetric analysis (TGA) instrument. For the TGA experiments, BTH (with 5 wt % H_2O added) or CHB−zirconia precursor mixtures were deposited onto a TGA pan followed by drying in vacuum to ensure that all the solvent was removed. The resulting residue was subjected to TGA analysis (10 °C/min). Attenuated total reflectance Fourier transform infrared (ATR-FTIR) spectra were acquired using a Thermo Nicolet Nexus 870 Fourier transform infrared spectrometer. Cross-sectional transmission electron microscopy (TEM) samples were prepared and imaged using a JEOL-2100F scanning/transmission electron microscope and a Hitachi HD-2300A scanning electron microscope, with both bright-field (BF) and high-angle annular dark-field (HAADF) detectors. The thicknesses of the CHB films were analyzed by profilometry (Veeco Dektak 150 surface profiler). The morphologies of all thin films were evaluated by atomic force microscopy (AFM) using a JEOL-5200 scanning probe microscope with silicon cantilevers operating in the tapping mode. MIS direct current measurements and OTFT measurements were carried out under ambient conditions using a Signatone probestation interfaced to a Keithley 6430 Sub-Femtoamp remote source meter and a Keithley 2400 source meter with a locally written LabVIEW program. An impedance analyzer (HP 4192A) was used for capacitance measurements.

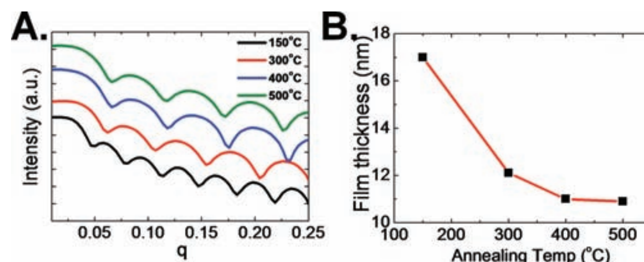

Figure 2. (A) XRR plots for ZrO_2 thin films fabricated on Si substrates and annealed at the indicated temperatures. (B) XRR-derived ZrO_2 film thicknesses as a function of the annealing temperature.

Results

The control ZrO_2 films and CHB dielectric films reported here consist of purely inorganic or inorganic plus organic components, respectively, with the latter containing various molar ratios of $ZrCl_4$ and organic α,ω-disilylalkane cross-linkers (Figure 1B). It will be seen that high-k ZrO_2 is the final inorganic component and that the cross-linkers function as binders between the organic and inorganic phases. Importantly, the spin-coated formulations of these two components result in smooth, robust, and mechanically flexible dielectric films at low processing temperatures (∼150 °C) and exhibit enhanced electrical insulating properties versus ZrO_2 films alone. Especially, they enable significantly reduced OTFT operating voltages (vide infra).

ZrO_2 Film Fabrication and Characterization. The control ZrO_2 dielectric films are prepared by spin-coating a solution of the appropriate inorganic precursor using the procedures described in the Experimental Section. To assess the influence of the ZrO_2 film annealing temperature, four different annealing temperatures (150, 300, 400, and 500 °C) were investigated after spin-coating the films. The X-ray reflectivity-derived thicknesses of the ZrO_2 films using 0.10 M Zr precursor solutions are ∼17.0, 12.1, 11.0, and 10.9 nm after 150, 300, 400, and 500 °C annealing, respectively (Figure 2). Clearly higher annealing temperatures (>400 °C) afford thinner, more dense films. For solution-processed metal oxide films, it is known that metal hydroxides are progressively converted to the oxides via thermally driven condensation processes (e.g., ≡Zr−OH + OH−Zr≡ → ≡Zr−O−Zr≡ + H_2O) and that the extent of oxide formation depends primarily on the annealing temperature.[10] The phase nature of the present sol−gel-derived ZrO_2 films was confirmed by GIXRD measurements. Figure 3 shows GIXRD patterns obtained for ZrO_2 films on Si annealed at 150, 300, 400, and 500 °C for 30 min. For the ZrO_2 films annealed at

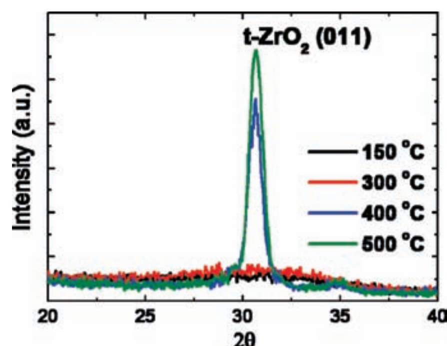

Figure 3. Glancing incidence X-ray diffraction patterns obtained from ZrO_2 layers annealed at 150, 300, 400, and 500 °C.

lower annealing temperatures (≤300 °C), the X-ray diffraction profiles exhibit broad amorphous-like features located at around $2\theta = 30°$. However, the peak shapes and intensities change substantially at higher annealing temperatures (400 and 500 °C), with the higher annealing temperatures yielding a sharp crystalline Bragg reflection at $2\theta = 30.3°$. Under these annealing conditions, it is expected that ZrO_2 will grow as the tetragonal phase, which is more favored at 400−700 °C than the monoclinic phase,[11] and the feature at $2\theta = 30.3°$ can be attributed to the (011) reflection of the tetragonal zirconia phase, which has a larger dielectric constant.[12] Using full width at half-maximum analysis of the $2\theta = 30.3°$ reflection and the Debye−Scherrer formula,[13] the average crystallite size for the present sol−gel-derived ZrO_2 films grown on Si is estimated to be ∼2 nm after annealing at 400−500 °C.

The amorphous or crystalline nature of the ZrO_2 films at various annealing temperatures is further confirmed by TEM. Parts A and B of Figure 4 show cross-section TEM images for 500 °C and 150 °C annealed ZrO_2 films, respectively. The thickness estimations are in good agreement with the XRR results. Nanobeam electron diffraction which can collect diffraction patterns from a nanoscale area (i.e., 20 nm in diameter) was used to identify the phase, as shown as the insets in Figures 4A,B. The nanodiffraction patterns of the ZrO_2 films annealed at 150 °C have a diffuse amorphous ring structure, while the ZrO_2 films annealed at 500 °C can be indexed in the tetragonal ZrO_2 crystalline phase. These data demonstrate that the ZrO_2 films at low annealing temperatures (<300 °C) are essentially amorphous whereas the ZrO_2 films subjected to higher annealing temperatures (>400 °C) are crystalline, in agreement with the GIXRD experiments. Additional TEM images after annealing at various temperatures are presented in the Supporting Information.

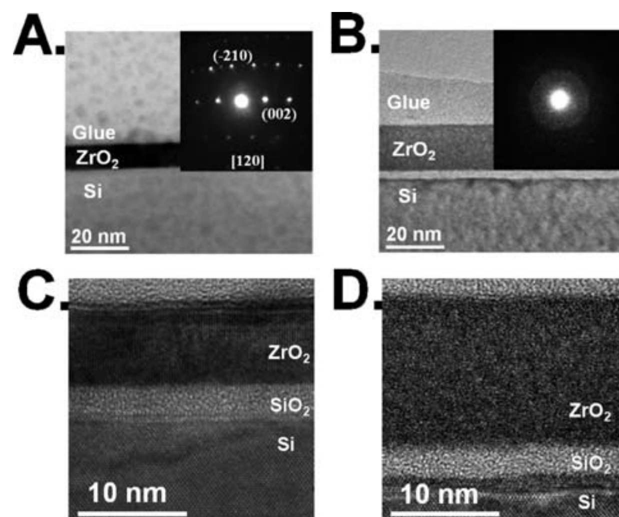

Figure 4. (A) Low-magnification STEM image of the Si interface of a film annealed at 500 °C. Labels indicate the layer identities. The inset shows the corresponding [120] nanodiffraction pattern of the crystalline tetragonal ZrO_2 layer. (B) TEM image of the $Si/SiO_2/ZrO_2$ interface of the film annealed at 150 °C. Labels indicate the layer identities. The inset shows the corresponding nanodiffraction pattern with a diffuse amorphous ring. (C, D) High-resolution TEM images of the $Si/SiO_2/ZrO_2$ interfaces of films annealed at 500 °C and 150 °C, respectively.

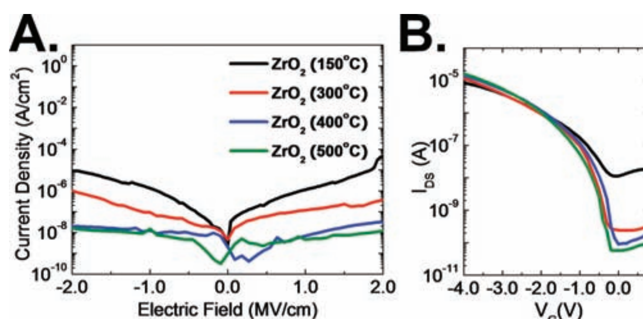

Figure 5. (A) Leakage current density vs electrical field for ZrO_2 dielectric films annealed at temperatures of 150 °C (black), 300 °C (red), 400 °C (blue), and 500 °C (green). (B) Transfer plots for pentacene OTFTs based on the ZrO_2 dielectric films of panel A.

To quantify the ZrO_2 dielectric properties, MIS sandwich structures were fabricated using vapor-deposited 200 μm × 200 μm Au contacts on dielectric-coated Si substrates. Figure 5A shows typical current density versus electric field ($J-E$) plots for MIS structures fabricated with the ZrO_2 dielectric films annealed at increasing temperatures. The leakage current density of these films progressively decreases as the annealing temperature is increased. Furthermore, high annealing temperatures (≥300 °C) are required to obtain adequate dielectric strength (<10^{-6} A/cm^2 at 2 MV/cm) for efficient OTFT operation (vide infra). The data are summarized in Table 1. The ZrO_2 dielectric in the n^+-Si/dielectric/Au MIS devices can be modeled as two capacitors in series, $1/C_i = 1/C_{ZrO_2} + 1/C_{SiO_2}$. The capacitance of the native oxide on the Si bottom electrode is 1380 nF/cm^2 assuming a 2.5 nm thick (from the TEM image) SiO_2 layer and $k = 3.9$. The C_i of the ZrO_2 is measured as 395−700 nF/cm^2, yielding a dielectric constant of 11−17, depending on the particular annealing temperature. The dielectric constants obtained for ZrO_2 are somewhat smaller than in bulk, highly

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Table 1. Summary of Dielectric and Film Properties for ZrO_2 and Cross-Linked Hybrid Blend Dielectrics[a]

dielectric film	cross-linker	Zr:cross-linker molar ratio	T_a [b] (°C)	film thickness (nm)	J (A/cm^2) at 2 MV/cm	ε
ZrO_2	none	1:0	150	17.0	$\sim 5 \times 10^{-5}$	10.8
			300	12.1	$\sim 1 \times 10^{-6}$	13.2
			400	11.0	$\sim 3 \times 10^{-8}$	17.5
			500	10.9	$\sim 2 \times 10^{-8}$	17.7
CBTH	BTH	1:0.5		35	$\sim 4 \times 10^{-7}$	5.9
		1:0.2	150	23	$\sim 1 \times 10^{-6}$	8.9
		1:0.1		19	$\sim 4 \times 10^{-6}$	10.2
CBTO	BTO	1:0.5		43	$\sim 1 \times 10^{-6}$	5.0
		1:0.2	150	27	$\sim 3 \times 10^{-6}$	7.1
		1:0.1		20	$\sim 6 \times 10^{-6}$	10.1

[a] Measured on MIS structures. [b] T_a = annealing temperature.

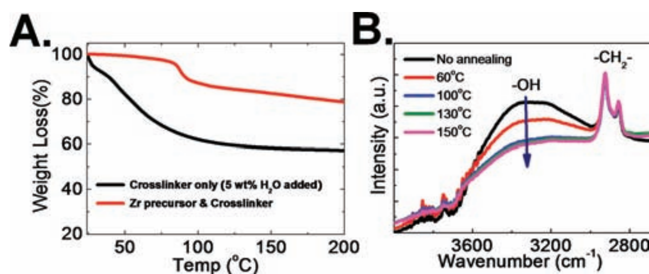

Figure 6. (A) TGA curves of a single component (BTH cross-linker) and mixed components (BTH−Zr precursor). (B) ATR-FTIR spectra of CBTH films as a function of annealing temperature.

crystalline zirconia or in thick films (16−25),[8] and the present films are likely less dense than those grown using more elaborate high-vacuum and high-temperature techniques.[14]

Cross-Linked Hybrid Dielectric Film Fabrication and Characterization. The new CHB dielectric films (Figure 1B) are prepared by spin-coating a solution of a zirconium oxide sol−gel solution combined with either of two different organosilane cross-linking reagents (Figure 1B) using the procedures described in the Experimental Section. This procedure yields 20−43 nm thick films as established by profilometry. Films of greater thicknesses, if required, can be obtained by varying the processing conditions or by multiple spin-on depositions since the CHBs are insoluble in the mother solutions at all stages of curing. In this chemistry, a CHB dielectric network is formed by condensation of the zirconia gel and the moderately reactive $-Si(OR)_3$ groups of the cross-linking reagents. Previous all-organic cross-linked polymer blends (CPBs) based on chlorosilane cross-linkers afford relatively rough dielectric film surfaces due to the high reactivity of chlorosilanes, and alternative cross-linkers affording smoother film morphologies were subsequently developed.[4b] In the present investigation, the relatively slow condensation between the cross-linker alkoxy groups and the zirconia gel hydroxyl groups results in smooth, dense, and robust CHB films with excellent leakage current properties. Figure 6 shows the thermal behavior of the BTH cross-linker and of a BTH−Zr precursor mixture as determined by TGA. For the cross-linker component alone, the broad weight loss occurring between 50 and 125 °C can be attributed to methanol loss, resulting from slow CHB consensation−cross-linking. In the case of the two-component mixture, the abrupt weight loss observed at ~90 °C is assigned to methanol evaporation after efficient cross-linking. These data suggest that far more acidic ZiO_x catalyzes the condensation/polymerization chemistry,

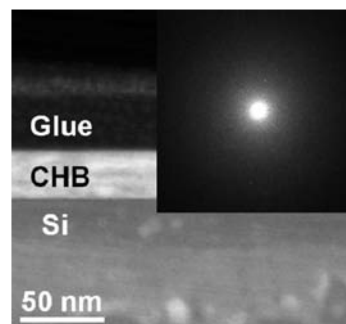

Figure 7. Cross-section TEM image of the Si/SiO_2/CHB (1:0.5 ratio) interface of a film annealed at 150 °C. Labels indicate the layer identities. The inset shows the corresponding nanodiffraction pattern with a diffuse amorphous ring.

which is essentially complete by ~90 °C. This result is supported by ATR-FTIR experiments carried out on CBTH films annealed at different temperatures. As shown in Figure 6B, the intensity of the Zr−OH stretching mode (~3300 cm^{-1}) decreases when the temperature is increased to ~100 °C and then stabilizes. These data clearly demonstrate that CHB cross-linking is complete by 150 °C. Figure 7 shows cross-section scanning transmission electron microscopy (STEM) images for a 150 °C annealed ZrO_2-based CHB film collected by the annular dark-field detector, which shows z contrast. Thickness measurements are in good agreement with the profilometry results, and the nanodiffraction patterns of the CHB film annealed at 150 °C have a diffuse amorphous ring structure. These data demonstrate that the CHB films processed at low annealing temperatures are essentially amorphous, similar to the ZrO_2 films subjected to low annealing temperatures (150 °C).

To assess the influence of a CHB microstructure on dielectric properties (Figure 1), two different cross-linkers, BTH and BTO, and three different $ZrCl_4$:cross-linker molar ratios (1:0.5, 1:0.2, and 1:0.1) were investigated in CHB film fabrication. It will be seen that this process affords materials with properties substantially different from those of neat ZrO_2 films of similar or greater thicknesses and which are characterized here by AFM, as well as by MIS structure leakage current and capacitance measurements. When a new cross-linker is employed, it is necessary to optimize the Zr:cross-linker molar ratio. The goal is to achieve, for a specific film thickness range, maximum capacitance along with smooth dielectric surfaces. Since a smooth dielectric/semiconductor interface is a prerequisite for efficient charge mobility in the TFT channel, AFM data provide important information on surface roughness for initial material evaluation.[15] Table 1 summarizes the dielectric properties of 20−43 nm thick CHB films prepared with different zirconium precursor:cross-linker molar ratios. Figure 8 shows AFM images of CBTH- and CBTO-derived films prepared from $ZrCl_4$ and the indicated cross-linkers. Independent of the $ZrCl_4$:cross-linker molar ratio, BTH is found to be a more effective cross-linking reagent, affording very smooth CBTH surfaces (rms roughness $\rho \approx 0.2$ nm). In contrast, BTO cross-linker-derived dielectric films are found to be relatively rough ($\rho = 0.6-5$ nm). BTO has a more extended hydrocarbon linker, offering greater degrees of motional freedom than that of BTH, and this phenomenon

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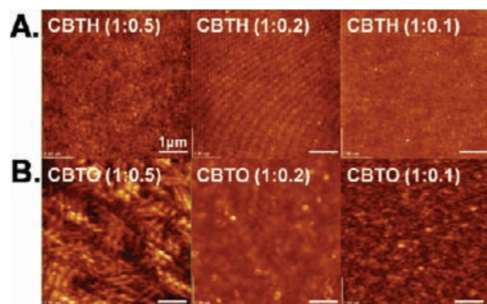

Figure 8. AFM images of CHB dielectric films as a function of the indicated $ZrCl_4$:cross-linker molar ratio and using either BTH (A) or BTO (B) as the cross-linker. The space bar indicates 1 μm.

affords relatively rougher CBTO surfaces, with smoother CBTO films obtained at lower BTO cross-linker concentrations.

Capacitance and leakage current density measurements (Figure 9) were next performed on these MIS structures. CBTH and CBTO films fabricated with BTH and BTO afford at least 10× lower leakage current densities (<1 × 10^{-6} A/cm^2) than the ZrO_2 films (~1 × 10^{-5} A/cm^2) at the same bias window (2 MV/cm). As the cross-linker content is increased, the leakage current density falls. This is the result of the improved network-forming capacity, affording denser films versus the inorganic-only films when annealed at low temperatures. Note, however, that capacitance *vs*. voltage ($C-V$) measurements reveal that increased cross-linker contents depress the film capacitance. This is the result of dilution of the ZrO_x content (expected from effective medium theory[3b,6a]) of the blend as well as increased film thickness. Nevertheless, capacitances in the range 95−365 nF/cm^2, far greater than that of a 300 nm thick thermal SiO_2 layer (~11 nF/cm^2), are readily achieved. From the accumulation regime capacitances, k values of 5.0−10.2 are obtained for the various cross-linkers and cross-linker molar ratios. These metrics compare favorably with inorganic dielectric materials typically used in OTFTs and are superior to those of conventional SiO_2 (k = 3.9) and a great many polymer/inorganic nanoparticle nanocomposite films.[6] Since the present CHB films exhibit excellent dielectric properties, they were next investigated as gate dielectrics in archetypical OTFTs.

Pentacene Thin-Film Transistor Fabrication and Characterization. Bottom-gate top-contact pentacene OTFTs were next fabricated using both neat ZrO_2 and the CHB films as the gate dielectrics, as described in the Experimental Section. From the $I-V$ data, the average pentacene field-effect mobility is calculated in the saturation regime ($V_G < V_{DS} = -4.0$ V) by plotting the square root of the drain current versus gate voltage (eq 1). Figure 5B shows representative transfer plots for pentacene OTFTs fabricated with the neat ZrO_2 control dielectric films which were annealed at various temperatures in the range 150−500 °C. Note that these devices require annealing of the dielectric at or above 300 °C to function properly. Thus, when the ZrO_2 dielectric films are annealed from 150 to 500 °C, the TFT hole mobility increases from 0.1 to 0.4 cm^2/(V·s). OTFTs were next fabricated on the various CHBs again using pentacene as the active semiconducting layer. In contrast to the above ZrO_2 results, pentacene TFTs fabricated with the CHB dielectric films all exhibit excellent linear and saturation regime characteristics and minimal hysteresis when operated at −4.0 V. Furthermore, since all of these dielectric films are very smooth, the device yields approach 98% (39 out of 40) with very narrow device performance spreads and with essentially every device performing similarly. The transistor performance characteristics of these devices are collected in Table 2. Figure 10 shows representative transfer plots for OTFTs fabricated with the CBTH gate dielectric annealed at 150 °C. Clearly these devices require far lower annealing temperatures to operate properly than those fabricated with the neat ZrO_2 films. Pentacene TFTs fabricated on CBTH ($ZrCl_4$:BTH = 1:0.5) exhibit exceptional device characteristics with a pentacene mobility of 1.5 cm^2/(V·s), a

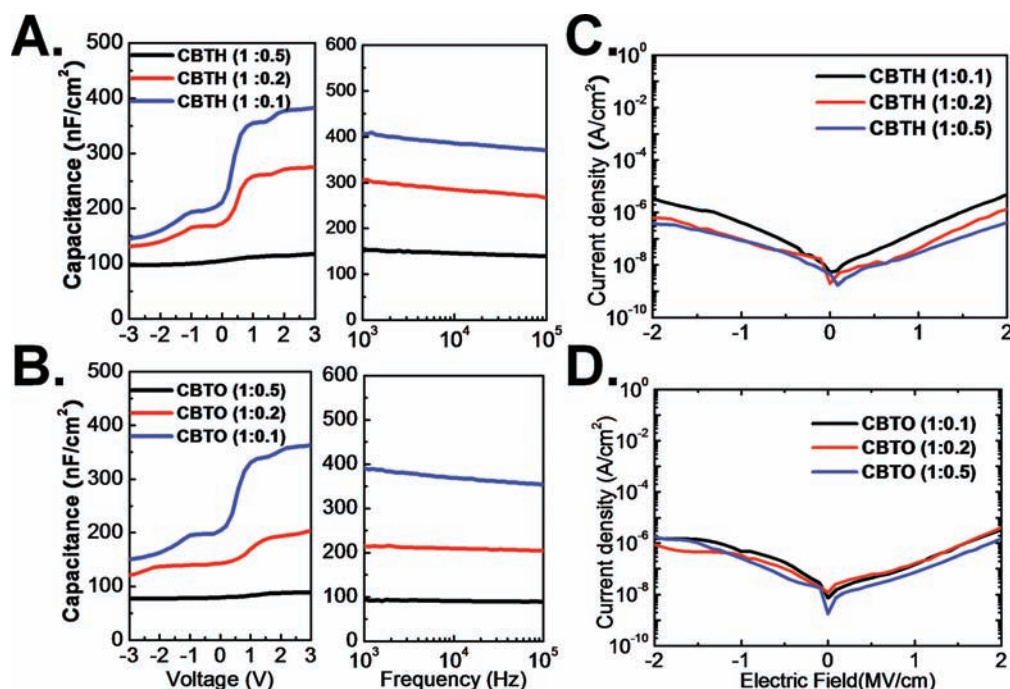

Figure 9. Capacitance vs voltage plots measured at 10 kHz (left) and capacitance vs frequency plots measured at 3.0 V (right) for CBTH (A) and CBTO (B) films. Leakage current density vs electric field plots for CBTH (C) and CBTO (D) films. The $ZrCl_4$:cross-linker molar ratios are indicated in the plot legends in parentheses.

Table 2. Zirconium Chloride:Cross-Linker Molar Ratio, Annealing Temperature (T_a, °C), Capacitance (C_i, nF/cm^2), Dielectric rms Roughness (ρ, nm), OTFT Carrier Mobility (μ_{sat}, cm^2/(V·s)), and Current On/Off Ratio (I_{on}/I_{off}) Data for MIS and OTFT Devices Fabricated Using Pentacene as the Organic Semiconductor and Various ZrO_2 and CHB Dielectrics

							P5		
dielectric film	cross-linker	substrate	Zr: cross-linker molar ratio	T_a	C_i	ρ	μ_{sat}	I_{on}/I_{off}	V_{TH}
ZrO_2	none	n^+-Si	1:0	150	395	0.2	0.1	10^4	−0.7
				300	567	0.2	0.3	10^5	−1.0
				400	700	0.2	0.4	10^5	−1.1
				500	700	0.2	0.4	10^5	−1.1
CBTH	BTH	n^+-Si	1:0.5		135	0.2	1.5	10^5	−1.2
			1:0.2	150	275	0.2	1.0	10^5	−1.1
			1:0.1		365	0.2	0.7	10^4	−1.0
CBTO	BTO	n^+-Si	1:0.5		95	0.6	0.2	10^3	−1.8
			1:0.2	150	200	1.3	0.3	10^4	−1.5
			1:0.1		345	5	0.6	10^4	−1.1
CBTH	BTH	Kapton/Al	1:0.5	150	132	0.2	1.6	10^5	−1.6

current on/off ratio of $\sim10^5$, and a threshold voltage of −1.2 V. In addition, the TFTs based on the CBTO gate dielectric exhibit good performance with μ approaching 0.6 cm^2/(V·s), a current on/off ratio of $\sim10^4$, and a threshold voltage of −1.1 V. These carrier mobilities are far larger than those of control devices fabricated with a conventional 300 nm thick SiO_2 gate dielectric (mobility ~0.3 cm^2/(V·s)). The operating voltage is only −4.0 V for the CHB-based devices vs −100 V for SiO_2 as a result of the greater capacitance of the CHB vs SiO_2 gate dielectric. The influence of the $ZrCl_4$:cross-linker molar ratio on transistor performance is also shown in Table 2. The optimal Zr:cross-linker molar ratio for CBTH is found to be 1:0.5 and for CBTO 1:0.1. For TFTs based on CBTH, when the $ZrCl_4$:cross-linker molar ratio is increased, the gate capacitance increases; however, the dielectric strength falls owing to the lower film density. Therefore, the TFT performance suffers as a result of the greater gate leakage. In contrast, the OTFT performance of the CBTO-based devices increases when the Zr:cross-linker molar ratios increase from 1:0.5 to 1:0.1 as a result of the smoother film morphology. Note that the threshold voltage variations of the devices based on different cross-linker:Zr precursor ratios are not due to different dielectric interface trap densities but are only the result of the different CBTH/CBTO capacitances due to dielectric thickness variations. Using a similar process, we also demonstrated an n-type organic transistor using a perylene diimide semiconductor (PDIF-CN_2) (see the Supporting Information, Figure S2, Table S1). These devices also operate at low voltages (<−4.0 V) and exhibit very large electron mobilities (up to 0.6 cm^2/(V·s)) and acceptable on/off current ratios (up to10^3).

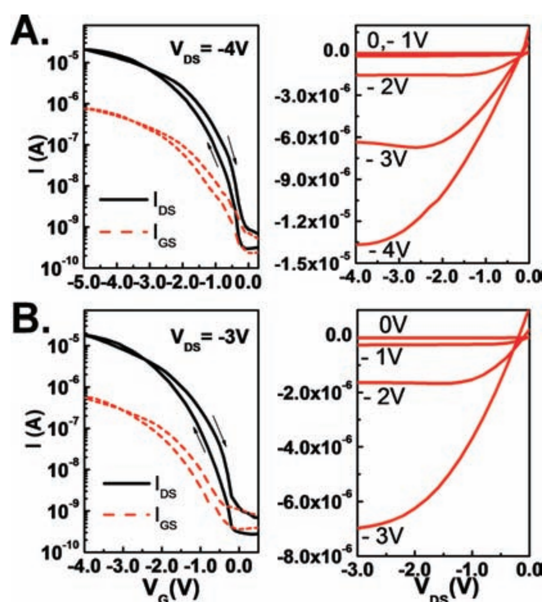

Figure 10. Transfer (left) and output (right) plots for pentacene OTFTs fabricated with the CHB gate dielectric using $ZrCl_4$:BTH cross-linker molar ratios of 1:0.5 (A) and 1:0.2 (B).

Figure 11 shows representative transfer and output plots for flexible pentacene TFTs based on CBTH (1:0.5 molar ratio) fabricated on the plastic substrate Kapton. These plots exhibit reproducible $I-V$ characteristics at low operating voltages (<−4.0 V) as well as excellent linear/saturation behavior. These flexible pentacene TFTs exhibit hole mobilities of 1.6 ± 0.2 cm^2/(V·s) and current on/off ratios of $\sim10^5$. These properties are quite comparable to those of TFTs fabricated on CBTH-coated silicon substrates. The data are summarized in Table 2.

Discussion

CHB Morphology and TFT Response Characteristics. All of the cross-linking reactions employed in this study yield robust, smooth, adherent, and insoluble CHB films. The major differences between the various CHBs involve details of film morphology (film roughness) originating from the different cross-linkers. Since OTFT charge transport is confined to the nanoscopic region at the semiconductor/dielectric interface, the smoothness of the dielectric film surface is clearly a prerequisite for optimizing the OTFT performance. In the case of pentacene TFTs, several groups have reported that rough gate dielectric surfaces induce the growth of smaller pentacene grains than in the case of very smooth substrates[16] and that roughness leads to a poor OTFT response. It is known that grain boundaries between crystallites are correlated with interfacial charge trapping sites which disrupt carrier drift.[17] Figures 12 and 13

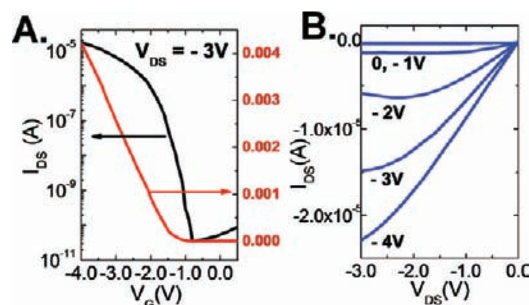

Figure 11. Transfer (A) and output (B) plots for representative flexible pentacene OTFTs fabricated with a CBTH gate dielectric on Kapton/aluminum substrates.

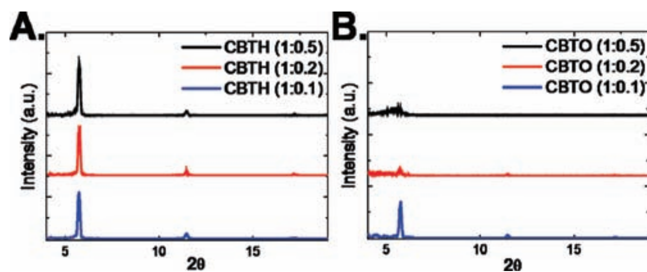

Figure 12. $\theta - 2\theta$ X-ray diffraction patterns of pentacene films grown on CBTH (A) and CBTO (B) dielectrics with the indicated $ZrCl_4$:cross-linker molar ratios.

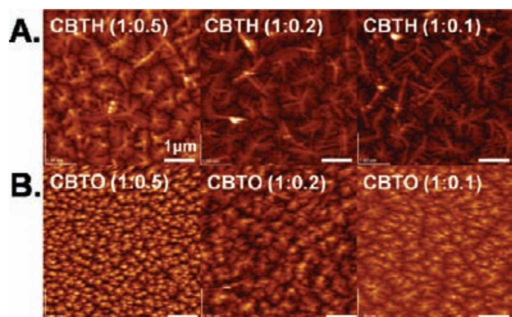

Figure 13. AFM images of pentacene films grown on CBTH (A) and CBTO (B) dielectrics prepared with the indicated $ZrCl_4$:cross-linker molar ratios. Images are of areas 5 μm × 5 μm in size.

show the XRD patterns and AFM images, respectively, of the pentacene films grown on CHB surfaces. The XRD data for pentacene films on CBTH-based dielectrics at all $ZrCl_4$:cross-linker ratios reveal the presence of the pentacene thin-film phase, characterized by the first reflection located at $2\theta = 5.7°$. Three characteristic features arising from the (00*l*) Bragg planes of the thin-film phase dominate the XRD patterns. These films are highly crystalline since the first reflection is sharp and intense. In contrast, pentacene films grown on rougher CBTO surfaces are far less textured. However, the film crystallinity increases as the BTO cross-linker concentration in the blend decreases, which affects the dielectric surface roughness. Rougher films are observed for CBTO vs CBTH, presumably because the more extended hydrocarbon linker offers greater degrees of motional freedom. Similar trends were observed for CPB dielectrics based on styrenic polymer/silane cross-linker mixtures.[4a] AFM images of pentacene films on each of the present CHB-based devices

Table 3. Device Parameters for the Flexible OTFTs Tested Before, During, and After Bending along a Curvature Parallel to the Channel Length

	ε_s[b] (%)	V_{DS} (V)	μ (cm^2/(V·s))	current on/off ratio	V_{TH} (V)
before bending		−3.0	1.5	10^5	−0.7
bending, r = 13 mm[a]	0.45	−3.0	1.2	10^5	−1.3
bending, r = 10 mm[a]	0.63	−3.0	0.7	10^4	−1.4
bending, r = 8 mm[a]	0.78	−3.0	0.3	10^4	−1.4
after bending		−3.0	1.3	10^4	−1.3

[a] r = bending radius. [b] ε_s = tensile strain, calculated from $\varepsilon_s \approx d_s/2r$, where d_s is the substrate thickness (= 125 mm for Kapton used in this study).

reveal similar trends in pentacene film grain size vs the CHB surface roughness. Rough gate dielectric surfaces are known to impede lateral pentacene molecular diffusion, affording smaller grain sizes versus growth on very smooth substrates, and in the present case drastically suppress ordered pentacene molecular nucleation.[16b]

OTFT Mechanical Flexibility. To investigate the mechanical properties of the present flexible TFTs, we performed bending tests in the longitudinal direction (i.e., along the channel transport axis) by measuring the electrical characteristics of the devices while wrapped around glass tubes having different circular cross-sections, as shown in Figure 14C. This test evaluates the TFT performance before, during, and after bending. To induce maximum tensile strain (ε_s)[18] during bending, a relatively thick (~125 μm) Kapton substrate was used in fabrication. Parts A−C of Figure 14 show the transfer characteristics and $I_{DS}^{1/2}-V_G$ plots of identical devices tested before, during, and after bending, and performance parameters are compiled in Table 3. As shown in Figure 14C, the channel direction is oriented parallel to the bending direction. The effective device mobilities were evaluated at calculated strains of 0.45%, 0.63%, and 0.78%, which correspond to bend radii of 13, 10, and 8 mm, respectively. When the device is bent at $\varepsilon_s = 0.45\%$ (r = 13 mm), I_{on} decreases slightly, along with a slight decrease in μ. Further bending to larger ε_s values of 0.63% (r = 10 mm) and 0.78% (r = 8 mm) significantly alters the performance and leads to decreases in both I_{on} and μ. Such bending induces strain in pentacene devices, which can alter the intrinsic mobility, as is well-known.[19] Note that performance is almost completely recovered after relaxation of the strain, similar to flexible carbon nanotubes, Si nanoribbons, and other

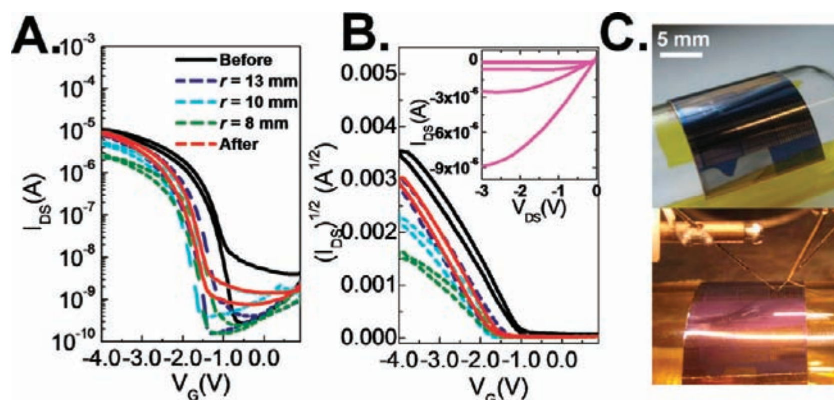

Figure 14. (A) Transfer characteristics and (B) $I_{DS}^{1/2}-V_G$ plots of flexible TFTs tested before, during, and after bending along a curvature parallel to the channel length. The legend indicates the bending radii employed. Inset: Output characteristics which are restored to the initial planar condition after bending. (C) Optical image of an array of OTFTs with CBTH (1:0.5) dielectric on a Kapton (125 mm thick) substrate, wrapped around a test tube with a radius of 8 mm, and image of the device during measurement.

organic transistors.[20] Remarkably, the after-bending device exhibits $I_{on} = 8.6 \times 10^{-6}$ A and $\mu = 1.3$ cm^2/(V·s) (85% of the original values). The performance loss is probably the result of degradation of the crystalline pentacene film order upon mechanical stress. This phenomenon has been observed in several studies where pentacene TFTs were fabricated on flexible substrates.[20f]

Conclusions

We have demonstrated here that blending *in situ* generated high-*k* inorganic materials with the appropriate difunctional organosilane cross-linking agents affords robust, smooth, adherent, flexible, insulating, pinhole-free, high-capacitance, ultrathin dielectric materials. These films are readily deposited from solution at low temperatures and adhere strongly to a variety of conducting substrates, including mechanically flexible plastics. The resulting OTFTs function at low operating voltages for an inorganic-based gate dielectric. These results demonstrate that low-leakage, high-capacitance, cross-linked inorganic/organic hybrid films are readily accessible and that OTFT devices implementing efficient, solution-process fabrication methodologies offer low voltage and low power operation.

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Supporting Information Available: Additional TEM images at various annealing temperatures and n-type organic transistor device performance data for chosen dielectric materials. This material is available free of charge via the Internet at http://pubs.acs.org.

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